



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,978	04/02/2001	Kevin J. McGrath	5500-66000	1318

7590 10/07/2004
Lawrence J. Merkel
Conley, Rose, & Tayon, P.C.
P.O. Box 398
Austin, TX 78767

EXAMINER

TSAI, HENRY

ART UNIT PAPER NUMBER

2183

DATE MAILED: 10/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/824,978

Applicant(s)

MCGRATH ET AL.

Examiner

Henry W.H. Tsai

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 July 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5, 7-15, 17-25 and 27-55 is/are pending in the application.
- 4a) Of the above claim(s) 31-41 and 43-55 is/are withdrawn from consideration.
- 5) ☐ Claim(s) is/are allowed.
- 6) ☒ Claim(s) 1-5, 7-15, 17-25, 27-30 and 42 is/are rejected.
- 7) ☐ Claim(s) is/are objected to.
- 8) ☐ Claim(s) are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s).
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7/20/04 6) ☐ Other:

Art Unit: 2183

DETAILED ACTION

Election/Restrictions

1. Newly submitted claim 31-41, and 43-53 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

This application contains claims directed to the following patentably distinct species of the claimed invention:

- I. The species best illustrated by claims 1-5, 7-15, 17-25, 27-30, and 42.
- II. The species best illustrated by claims 31-41.
- III. The species best illustrated by claims 43-53.

Currently, there's no generic.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 31-41, and 43-53 have been withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Art Unit: 2183

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-5, 7-15, 17-25, 27-30, and 42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 11-13, it is not clear what is meant by "a first address of a second instruction following the first instruction in the third register" because:

a. how to define "a first address" of a second instruction was not previously defined. Note the term "a first address of a second instruction" implies that the second instruction has at least a second address; and

b. It is not clear which element is in the third register, since "a first address", "a second instruction", or "the first instruction" may be in the third register.

Similar problems exist in claim 21.

In claim 11, lines 14-15, it is not clear what is meant by "a first address of a second instruction following the first instruction in the third storage" because:

Art Unit: 2183

- a. how to define "a first address" of a second instruction was not previously defined. Note the term "a first address of a second instruction" implies that the second instruction has at least a second address; and
- b. It is not clear which element is in the third storage since either "a first address", "the second instruction", or "the first instruction" may be in the third storage.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2183

5. Claims 1, 11, 21, and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Kogge (U.S. Patent No. 5,475,856), herein referred to as Kogge'856.

Referring to claim 1, Kogge'856 discloses as claimed a processor comprising: a first register (IR 105 in processor 1, see Fig. 3) configured to store a first target address (note instruction register IR inherently stores a fetched branch instruction containing a next instruction target address information); a second register (IR 105 in one of processors 2-N, see Fig. 3) configured to store a second target address (note as set forth above, instruction register IR inherently stores a fetched branch instruction containing a next instruction target address information); and an execution core (see Fig. 3, the processor comprising processors 1-N, see also col. 4, lines 38-40) coupled to the first register (IR 105 in processor 1, see Fig. 3) and the second register (IR 105 in one of processors 2-N, see Fig. 3), wherein the execution core is configured, responsive to a first instruction (see Col. 6, lines 21-22, and lines 38-40 when the processor 1 functions as a controller), to: (i) select the first target address from the first register (IR 105 in processor 1, see Fig. 3) as a next program counter address if a first operating mode (this is the situation when the SIMD mode is active, see Fig. 1a and see also col. 6, lines

Art Unit: 2183

34-37) is active in the processor, and (ii) select the second target address from the second register (IR 105 in one of processors 2-N, see Fig. 3) as the next program counter address if a second operating mode (this is the situation when the MIMD mode is active, see also col. 8, lines 52-56 regarding a processor (one of the processors 2-N, see Figs. 1b and 3), proceeds to fetch instructions as an individual processor) is active in the processor; and wherein the execution core is configured to store a first address (the next instruction address saved in PC 103 see Fig. 3 after the first instruction has been executed) of a second instruction following the first instruction in the third register (PC 103, see Fig. 3) responsive to the first instruction.

Referring to claim 11, Kogge'856 discloses as claimed an apparatus comprising: a first storage location (IR 105 in processor 1, see Fig. 3) corresponding to a first register, the first storage location storing a first target address (note instruction register IR inherently stores a fetched branch instruction containing a next instruction target address information); a second storage location (IR 105 in one of processors 2-N, see Fig. 3) corresponding to a second register, the second storage location storing a second target address (note as set forth above, instruction register IR inherently

Art Unit: 2183

stores a fetched instruction containing a next instruction target address information); and a processor (see Fig. 3, the processor comprising processors 1-N, see also col. 4, lines 38-40) coupled to the first storage location and the second storage location, wherein the processor is configured, responsive to a first instruction (see Col. 6, lines 21-22, and lines 38-40 when the processor 1 functions as a controller), to: (i) select the first target address from the first storage location (IR 105 in processor 1, see Fig. 3) as a next program counter address if a first operating mode (this is the situation when the SIMD mode is active, see Fig. 1a and see also col. 6, lines 34-37) is active, and (ii) select the second target address from the second storage location (IR 105 in one of processors 2-N, see Fig. 3) as the next program counter address if a second operating mode (this is the situation when the MIMD mode is active, see also col. 8, lines 52-56 regarding a processor (one of the processors 2-N, see Figs. 1b and 3), proceeds to fetch instructions as an individual processor) is active.

Referring to claim 21, Kogge'856 discloses as claimed a method comprising: selecting a first target address from a first register (IR 105 in processor 1, see Fig. 3) as a next program counter address responsive to a first operating mode (this is the situation when the SIMD mode is active, see Fig. 1a and see

Art Unit: 2183

also col. 6, lines 34-37) during execution of a first instruction (see Col. 6, lines 21-22, and lines 38-40 when the processor 1 functions as a controller); and selecting a second target address from a second register (IR 105 in one of processors 2-N, see Fig. 3) as the next program counter address responsive to a second operating mode (this is the situation when the MIMD mode is active, see also col. 8, lines 52-56 regarding a processor (one of the processors 2-N, see Figs. 1b and 3), proceeds to fetch instructions as an individual processor) during execution of the first instruction (since the first instruction in processor 1 determines either SIMD or MIMD mode, see also Col. 6, lines 21-22, and lines 38-40 when the processor 1 functions as a controller and col. 13, lines 25-27).

As to claim 42, Kogge'856 also discloses: a computer system (see Fig. 3) comprising the processor (1-N processors) and a peripheral device (a monitor of the Kogge'856's system) configured to communicate (through internet line) between the computer system and another computer system (such as a server or another computer system in the internet).

Art Unit: 2183

Allowable Subject Matter

6. Claims 2-5, 7-10, 12-15, 17-20, 22-25, and 27-30 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Amendment

7. Applicant's arguments filed 7/23/04 have been fully considered but they are not deemed to be persuasive.

"Request to Rescind Previous Non-Publication Request" has been entered.

Note the original claims 6 and 26 (now cancelled) each comprise a fourth register which has been interpreted as having a third register implicitly existing in the claim.

As set forth in the art rejections above, Kogge'856 anticipates the claimed invention

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS**

Art Unit: 2183

ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703)

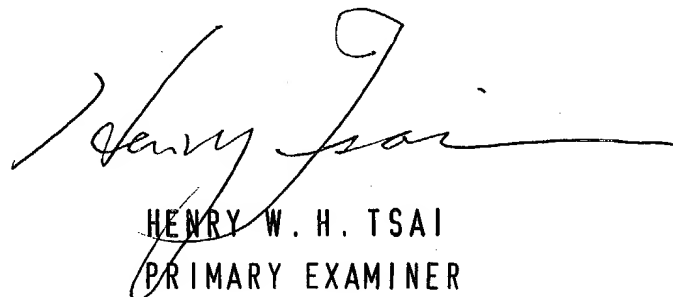
Art Unit: 2183

305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2100 receptionist whose telephone number is (703) 305-3900.

10. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into

the Group at fax number: 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.



HENRY W. H. TSAI
PRIMARY EXAMINER

October 4, 2004